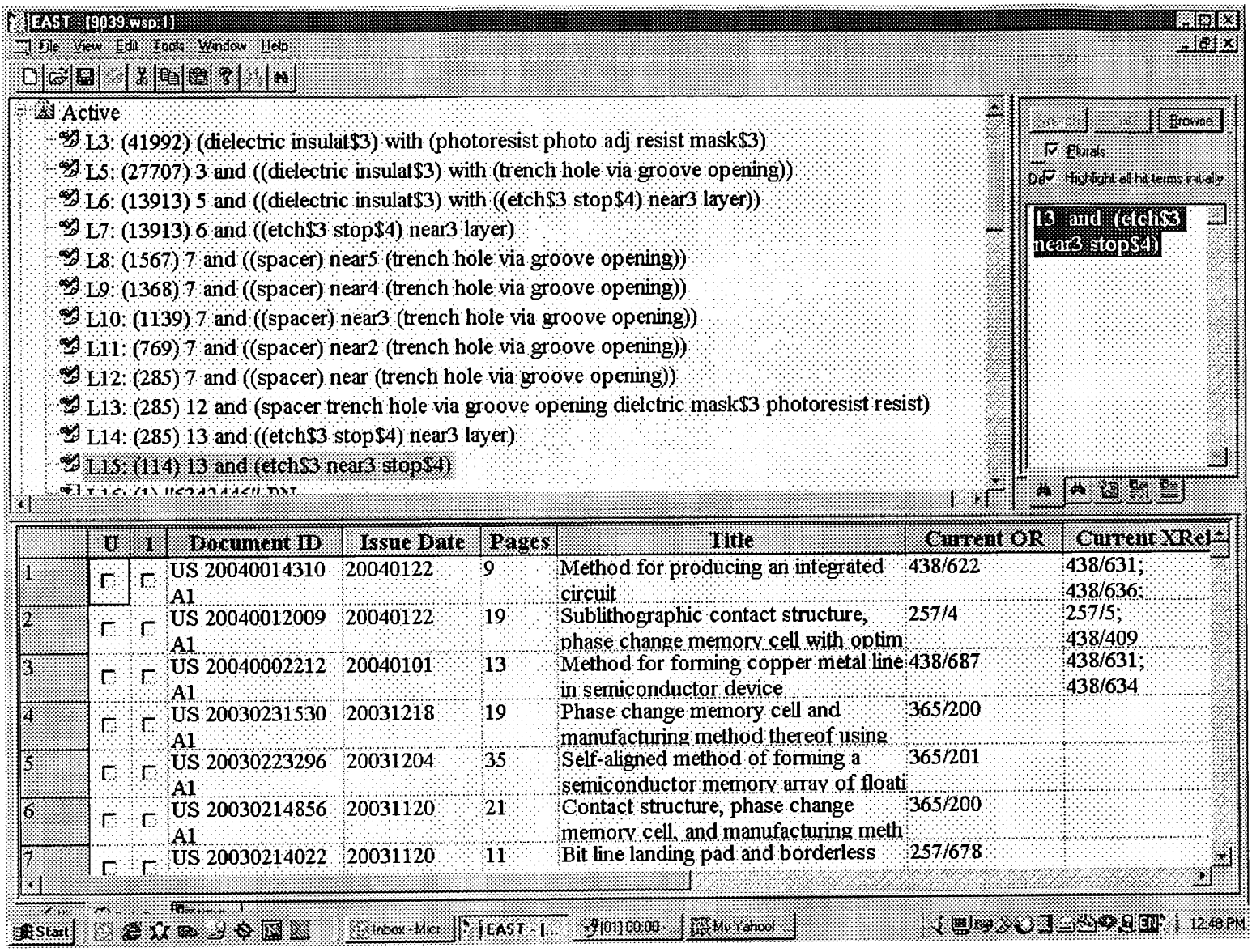
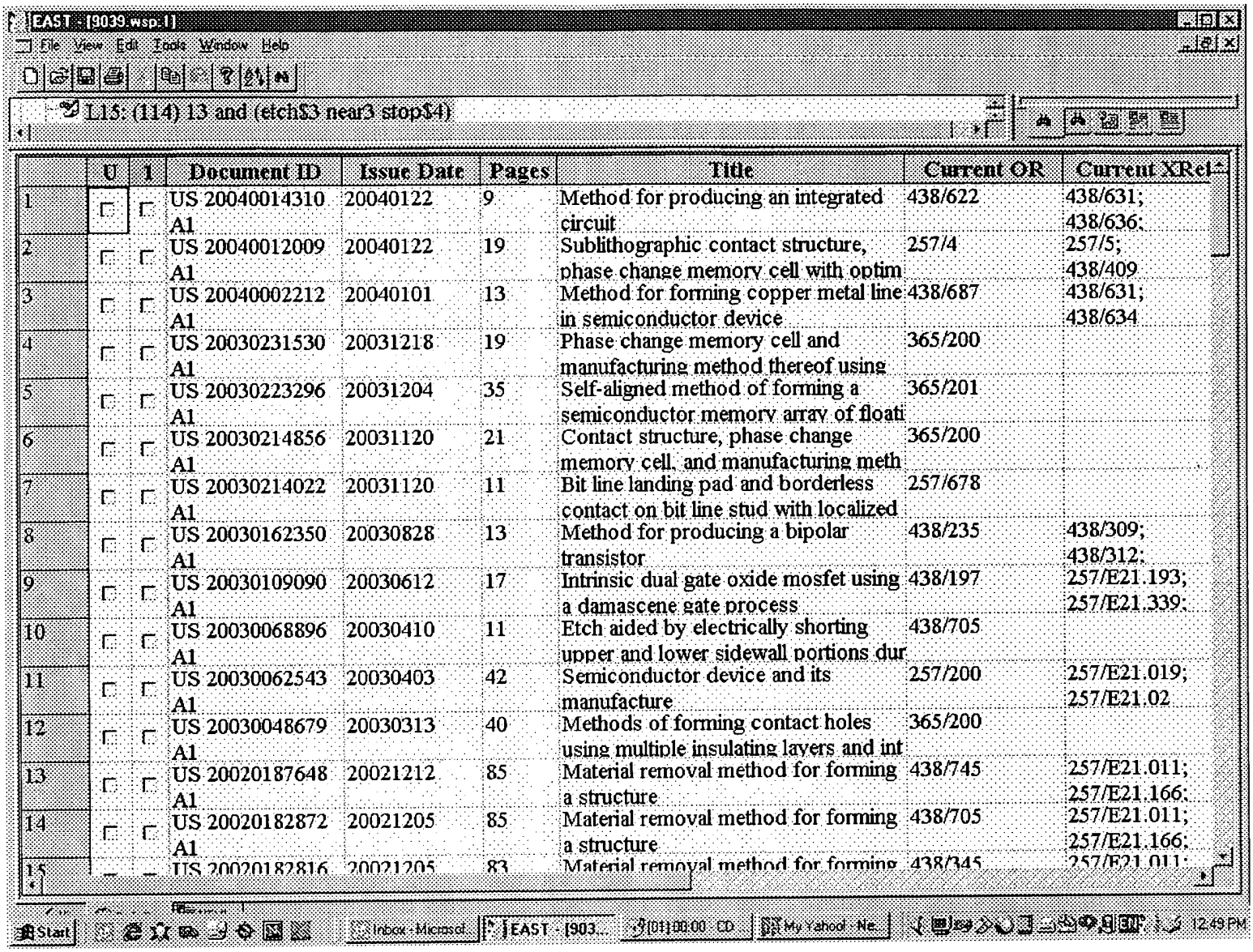
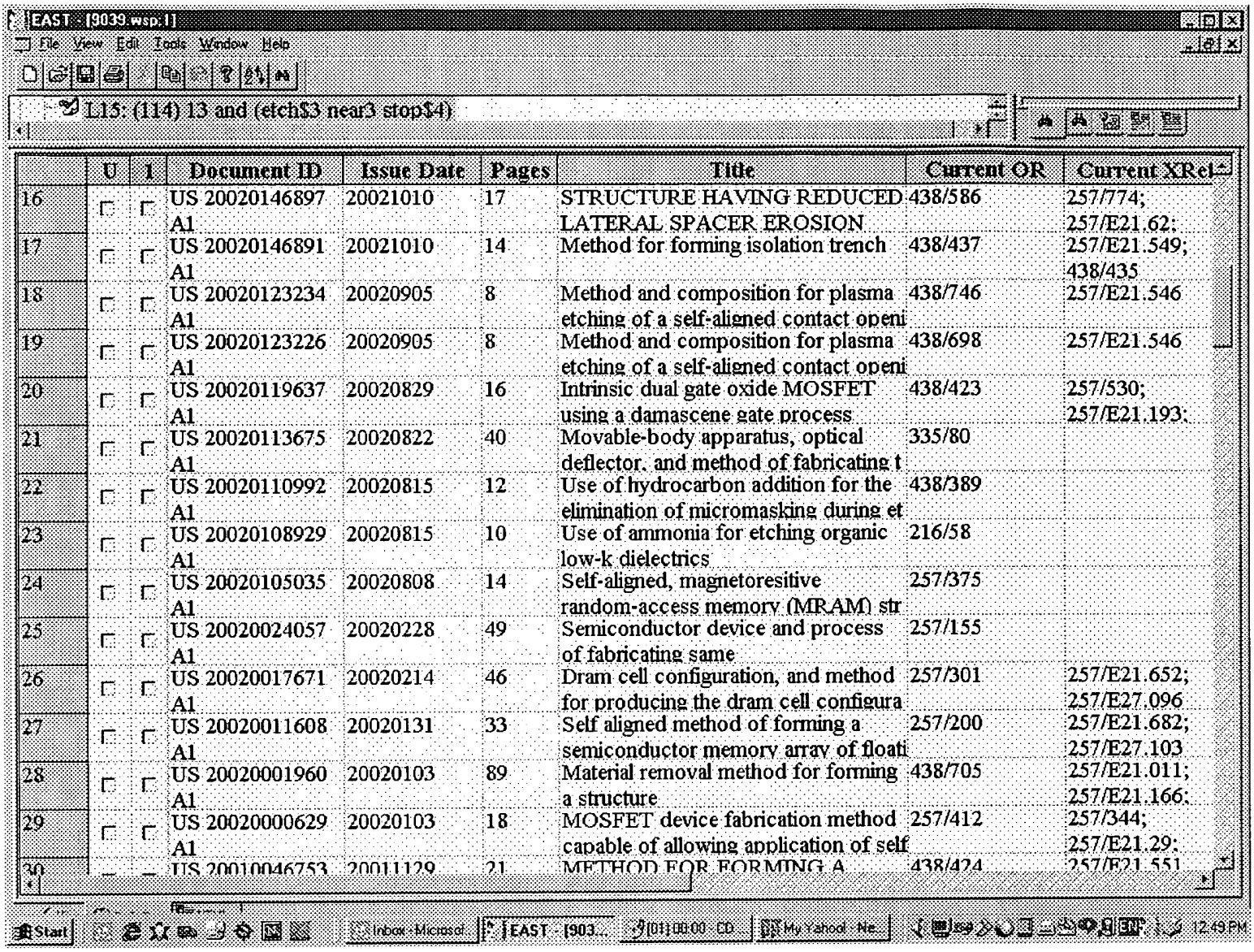


	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRel
1	☐	☐	US 20040014310 A1	20040122	9	Method for producing an integrated circuit	438/622	438/631; 438/636;
2	☐	☐	US 20040012009 A1	20040122	19	Sublithographic contact structure, phase change memory cell with optim	257/4	257/5; 438/409
3	☐	☐	US 20040002212 A1	20040101	13	Method for forming copper metal line in semiconductor device	438/687	438/631; 438/634
4	☐	☐	US 20030231530 A1	20031218	19	Phase change memory cell and manufacturing method thereof using	365/200	
5	☐	☐	US 20030223296 A1	20031204	35	Self-aligned method of forming a semiconductor memory array of floati	365/201	
6	☐	☐	US 20030214856 A1	20031120	21	Contact structure, phase change memory cell, and manufacturing meth	365/200	
7	☐	☐	US 20030214022	20031120	11	Bit line landing pad and borderless	257/678	



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRel
1	☐	☐	US 20040014310 A1	20040122	9	Method for producing an integrated circuit	438/622	438/631; 438/636;
2	☐	☐	US 20040012009 A1	20040122	19	Sublithographic contact structure, phase change memory cell with optim	257/4	257/5; 438/409
3	☐	☐	US 20040002212 A1	20040101	13	Method for forming copper metal line in semiconductor device	438/687	438/631; 438/634
4	☐	☐	US 20030231530 A1	20031218	19	Phase change memory cell and manufacturing method thereof using	365/200	
5	☐	☐	US 20030223296 A1	20031204	35	Self-aligned method of forming a semiconductor memory array of floati	365/201	
6	☐	☐	US 20030214856 A1	20031120	21	Contact structure, phase change memory cell, and manufacturing meth	365/200	
7	☐	☐	US 20030214022 A1	20031120	11	Bit line landing pad and borderless contact on bit line stud with localized	257/678	
8	☐	☐	US 20030162350 A1	20030828	13	Method for producing a bipolar transistor	438/235	438/309; 438/312;
9	☐	☐	US 20030109090 A1	20030612	17	Intrinsic dual gate oxide mosfet using a damascene gate process	438/197	257/E21.193; 257/E21.339;
10	☐	☐	US 20030068896 A1	20030410	11	Etch aided by electrically shorting upper and lower sidewall portions dur	438/705	
11	☐	☐	US 20030062543 A1	20030403	42	Semiconductor device and its manufacture	257/200	257/E21.019; 257/E21.02
12	☐	☐	US 20030048679 A1	20030313	40	Methods of forming contact holes using multiple insulating layers and int	365/200	
13	☐	☐	US 20020187648 A1	20021212	85	Material removal method for forming a structure	438/745	257/E21.011; 257/E21.166;
14	☐	☐	US 20020182872 A1	20021205	85	Material removal method for forming a structure	438/705	257/E21.011; 257/E21.166;
15	☐	☐	US 20020182816	20021205	83	Material removal method for forming	438/345	257/E21.011;



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
16	☐	☐	US 20020146897 A1	20021010	17	STRUCTURE HAVING REDUCED LATERAL SPACER EROSION	438/586	257/774; 257/E21.62;
17	☐	☐	US 20020146891 A1	20021010	14	Method for forming isolation trench	438/437	257/E21.549; 438/435
18	☐	☐	US 20020123234 A1	20020905	8	Method and composition for plasma etching of a self-aligned contact openi	438/746	257/E21.546
19	☐	☐	US 20020123226 A1	20020905	8	Method and composition for plasma etching of a self-aligned contact openi	438/698	257/E21.546
20	☐	☐	US 20020119637 A1	20020829	16	Intrinsic dual gate oxide MOSFET using a damascene gate process	438/423	257/530; 257/E21.193;
21	☐	☐	US 20020113675 A1	20020822	40	Movable-body apparatus, optical deflector, and method of fabricating t	335/80	
22	☐	☐	US 20020110992 A1	20020815	12	Use of hydrocarbon addition for the elimination of micromasking during et	438/389	
23	☐	☐	US 20020108929 A1	20020815	10	Use of ammonia for etching organic low-k dielectrics	216/58	
24	☐	☐	US 20020105035 A1	20020808	14	Self-aligned, magnetoresitive random-access memory (MRAM) str	257/375	
25	☐	☐	US 20020024057 A1	20020228	49	Semiconductor device and process of fabricating same	257/155	
26	☐	☐	US 20020017671 A1	20020214	46	Dram cell configuration, and method for producing the dram cell configura	257/301	257/E21.652; 257/E27.096
27	☐	☐	US 20020011608 A1	20020131	33	Self aligned method of forming a semiconductor memory array of floati	257/200	257/E21.682; 257/E27.103
28	☐	☐	US 20020001960 A1	20020103	89	Material removal method for forming a structure	438/705	257/E21.011; 257/E21.166;
29	☐	☐	US 20020000629 A1	20020103	18	MOSFET device fabrication method capable of allowing application of self	257/412	257/344; 257/E21.29;
30	☐	☐	US 20010046753	20011129	21	METHOD FOR FORMING A	438/424	257/E21.551

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
31	☐	☐	US 20010028077 A1	20011011	42	Semiconductor device and its manufacture	257/303	257/E21.019; 257/E21.02
32	☐	☐	US 20010024380 A1	20010927	43	Memory cell configuration in which an electrical resistance of a memory el	365/158	
33	☐	☐	US 20010019866 A1	20010906	13	Method of forming a contact hole in a semiconductor substrate using oxide	438/241	257/E21.257; 257/E21.577;
34	☐	☐	US 20010018787 A1	20010906	13	Method for fabricating a capacitor in a semiconductor memory device	29/25.01	216/18; 216/6;
35	☐	☐	US 6661823 B1	20031209	47	Vertical resonator type surface light emitting semiconductor laser device a	372/49	372/43; 372/45;
36	☐	☐	US 6620733 B2	20030916	12	Use of hydrocarbon addition for the elimination of micromasking during et	438/700	438/694; 438/710
37	☐	☐	US 6599840 B2	20030729	82	Material removal method for forming a structure	438/705	257/E21.011; 257/E21.166;
38	☐	☐	US 6596648 B2	20030722	83	Material removal method for forming a structure	438/745	257/E21.011; 257/E21.166;
39	☐	☐	US 6596642 B2	20030722	80	Material removal method for forming a structure	438/705	216/38; 216/87;
40	☐	☐	US 6586795 B2	20030701	44	DRAM cell configuration whose memory cells can have transistors an	257/302	257/303; 257/E21.652;
41	☐	☐	US 6559499 B1	20030506	7	Process for fabricating an integrated circuit device having capacitors with	257/311	257/309; 257/310;
42	☐	☐	US 6544861 B2	20030408	14	Method for forming isolation trench	438/424	257/E21.549; 438/296;
43	☐	☐	US 6537865 B2	20030325	47	Semiconductor device and process of fabricating same	438/172	
44	☐	☐	US 6531410 B2	20030311	16	Intrinsic dual gate oxide MOSFET using a damascene gate process	438/766	257/E21.193; 257/E21.339;
45	☐	☐	US 6521931 B2	20030218	14	Self-aligned, magnetoresitive	257/295	257/421

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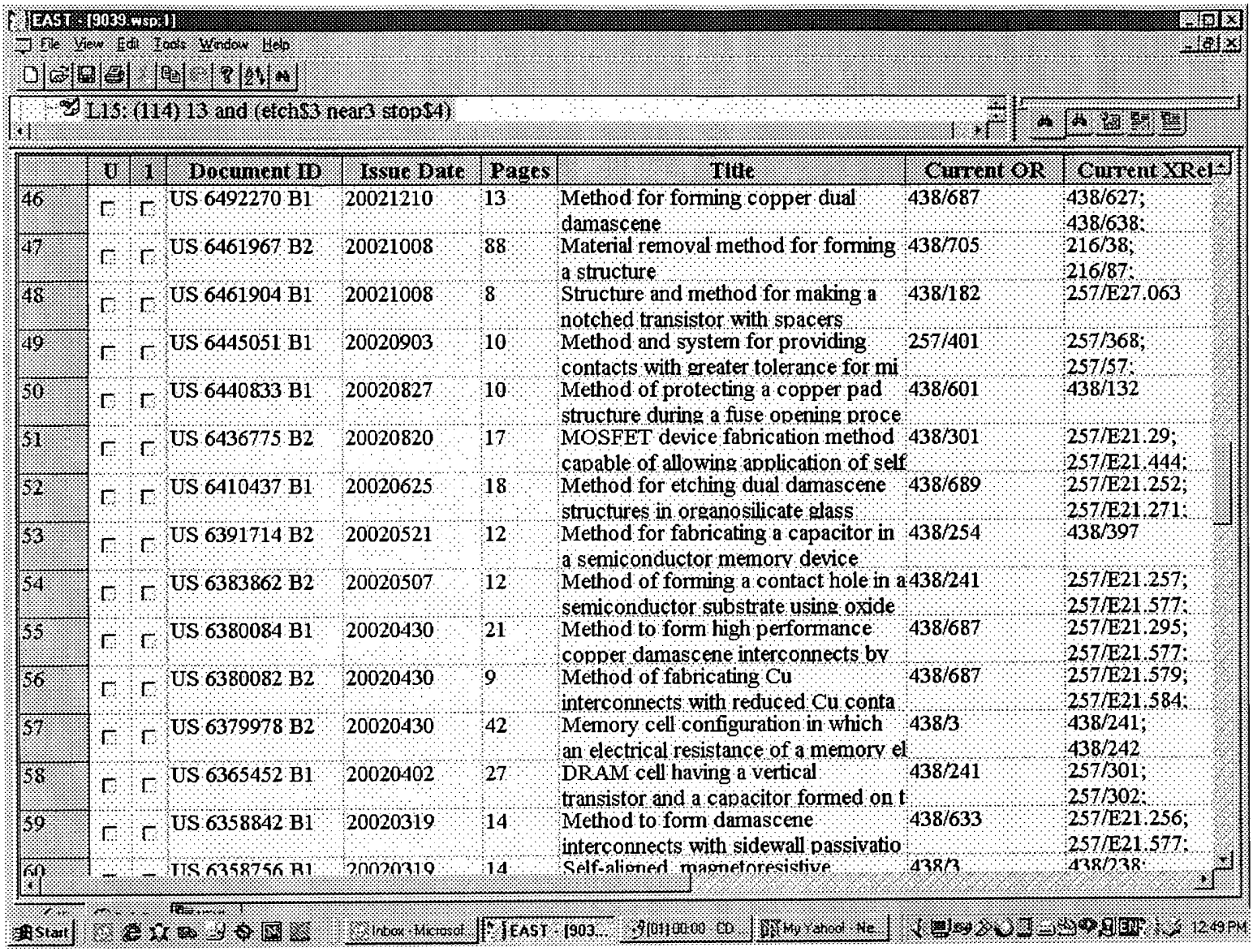
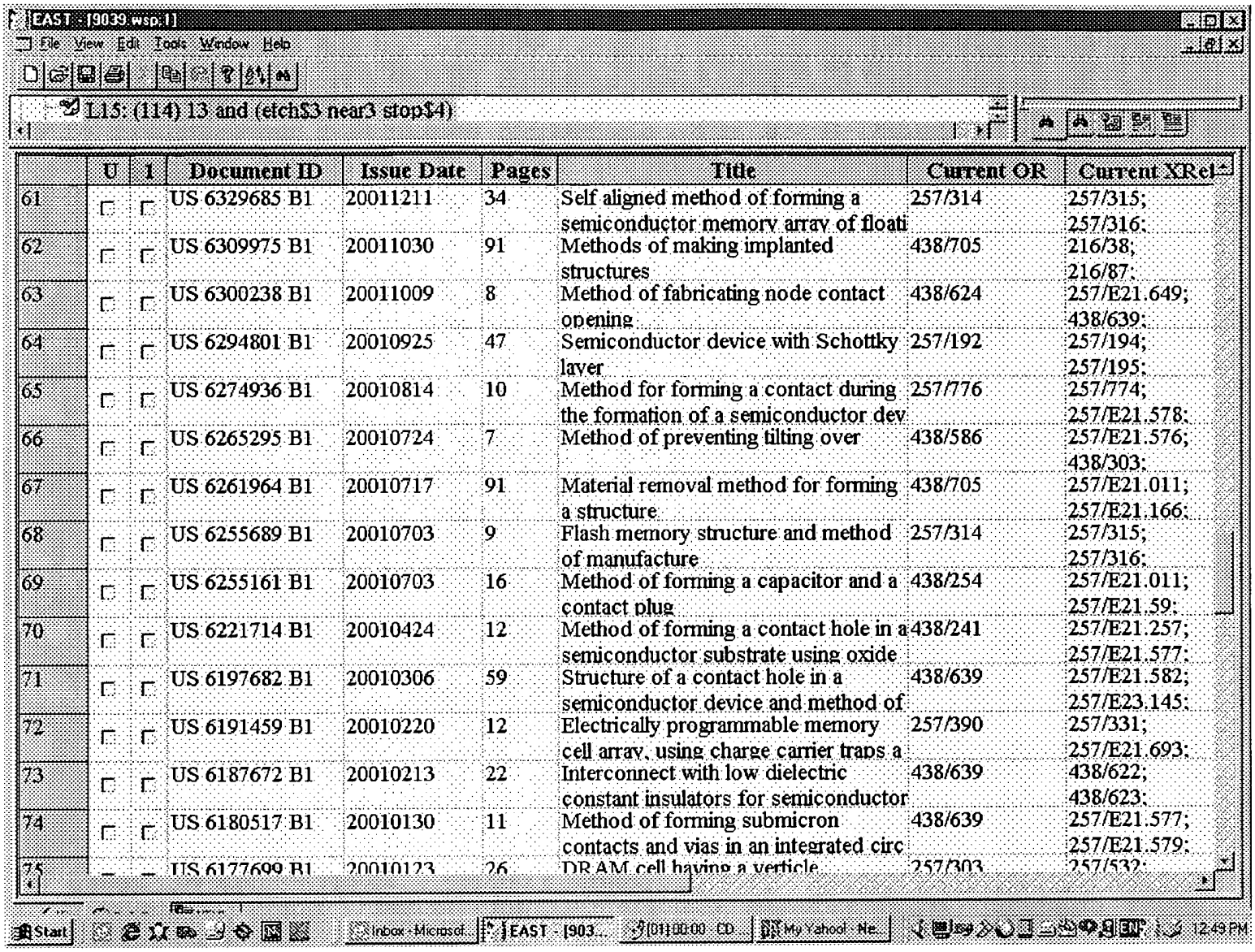
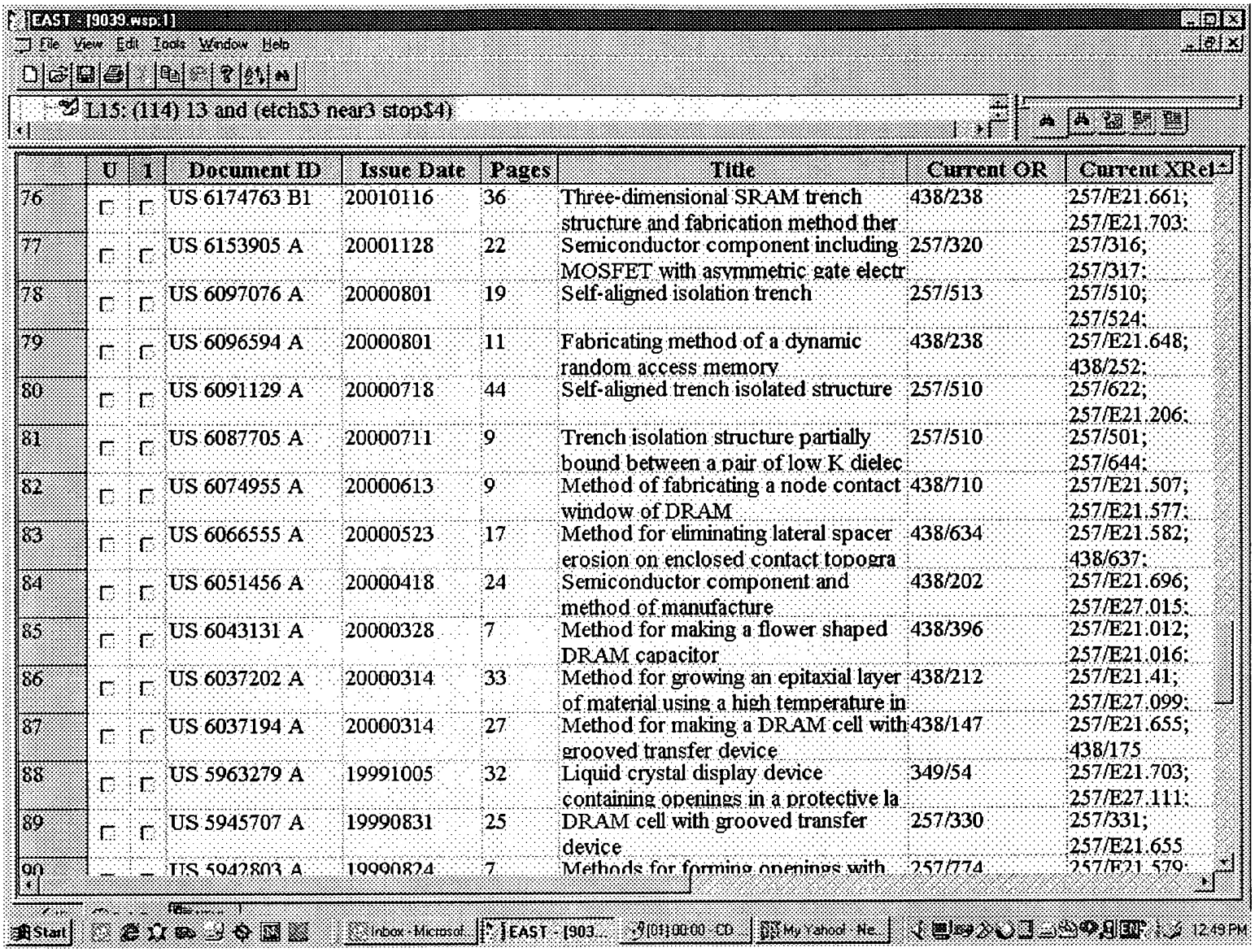


	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRel
46	☐	☐	US 6492270 B1	20021210	13	Method for forming copper dual damascene	438/687	438/627; 438/638;
47	☐	☐	US 6461967 B2	20021008	88	Material removal method for forming a structure	438/705	216/38; 216/87;
48	☐	☐	US 6461904 B1	20021008	8	Structure and method for making a notched transistor with spacers	438/182	257/E27.063
49	☐	☐	US 6445051 B1	20020903	10	Method and system for providing contacts with greater tolerance for mi	257/401	257/368; 257/57;
50	☐	☐	US 6440833 B1	20020827	10	Method of protecting a copper pad structure during a fuse opening proce	438/601	438/132
51	☐	☐	US 6436775 B2	20020820	17	MOSFET device fabrication method capable of allowing application of self	438/301	257/E21.29; 257/E21.444;
52	☐	☐	US 6410437 B1	20020625	18	Method for etching dual damascene structures in organosilicate glass	438/689	257/E21.252; 257/E21.271;
53	☐	☐	US 6391714 B2	20020521	12	Method for fabricating a capacitor in a semiconductor memory device	438/254	438/397
54	☐	☐	US 6383862 B2	20020507	12	Method of forming a contact hole in a semiconductor substrate using oxide	438/241	257/E21.257; 257/E21.577;
55	☐	☐	US 6380084 B1	20020430	21	Method to form high performance copper damascene interconnects by	438/687	257/E21.295; 257/E21.577;
56	☐	☐	US 6380082 B2	20020430	9	Method of fabricating Cu interconnects with reduced Cu conta	438/687	257/E21.579; 257/E21.584;
57	☐	☐	US 6379978 B2	20020430	42	Memory cell configuration in which an electrical resistance of a memory el	438/3	438/241; 438/242
58	☐	☐	US 6365452 B1	20020402	27	DRAM cell having a vertical transistor and a capacitor formed on t	438/241	257/301; 257/302;
59	☐	☐	US 6358842 B1	20020319	14	Method to form damascene interconnects with sidewall passivatio	438/633	257/E21.256; 257/E21.577;
60	☐	☐	US 6358756 B1	20020319	14	Self-aligned magnetoresistive	438/3	438/238;



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
61	☐	☐	US 6329685 B1	20011211	34	Self aligned method of forming a semiconductor memory array of floati	257/314	257/315; 257/316;
62	☐	☐	US 6309975 B1	20011030	91	Methods of making implanted structures	438/705	216/38; 216/87;
63	☐	☐	US 6300238 B1	20011009	8	Method of fabricating node contact opening	438/624	257/E21.649; 438/639;
64	☐	☐	US 6294801 B1	20010925	47	Semiconductor device with Schottky layer	257/192	257/194; 257/195;
65	☐	☐	US 6274936 B1	20010814	10	Method for forming a contact during the formation of a semiconductor dev	257/776	257/774; 257/E21.578;
66	☐	☐	US 6265295 B1	20010724	7	Method of preventing tilting over	438/586	257/E21.576; 438/303;
67	☐	☐	US 6261964 B1	20010717	91	Material removal method for forming a structure	438/705	257/E21.011; 257/E21.166;
68	☐	☐	US 6255689 B1	20010703	9	Flash memory structure and method of manufacture	257/314	257/315; 257/316;
69	☐	☐	US 6255161 B1	20010703	16	Method of forming a capacitor and a contact plug	438/254	257/E21.011; 257/E21.59;
70	☐	☐	US 6221714 B1	20010424	12	Method of forming a contact hole in a semiconductor substrate using oxide	438/241	257/E21.257; 257/E21.577;
71	☐	☐	US 6197682 B1	20010306	59	Structure of a contact hole in a semiconductor device and method of	438/639	257/E21.582; 257/E23.145;
72	☐	☐	US 6191459 B1	20010220	12	Electrically programmable memory cell array, using charge carrier traps a	257/390	257/331; 257/E21.693;
73	☐	☐	US 6187672 B1	20010213	22	Interconnect with low dielectric constant insulators for semiconductor	438/639	438/622; 438/623;
74	☐	☐	US 6180517 B1	20010130	11	Method of forming submicron contacts and vias in an integrated circ	438/639	257/E21.577; 257/E21.579;
75	☐	☐	US 6177699 B1	20010123	26	DRAM cell having a verticle	257/303	257/532;



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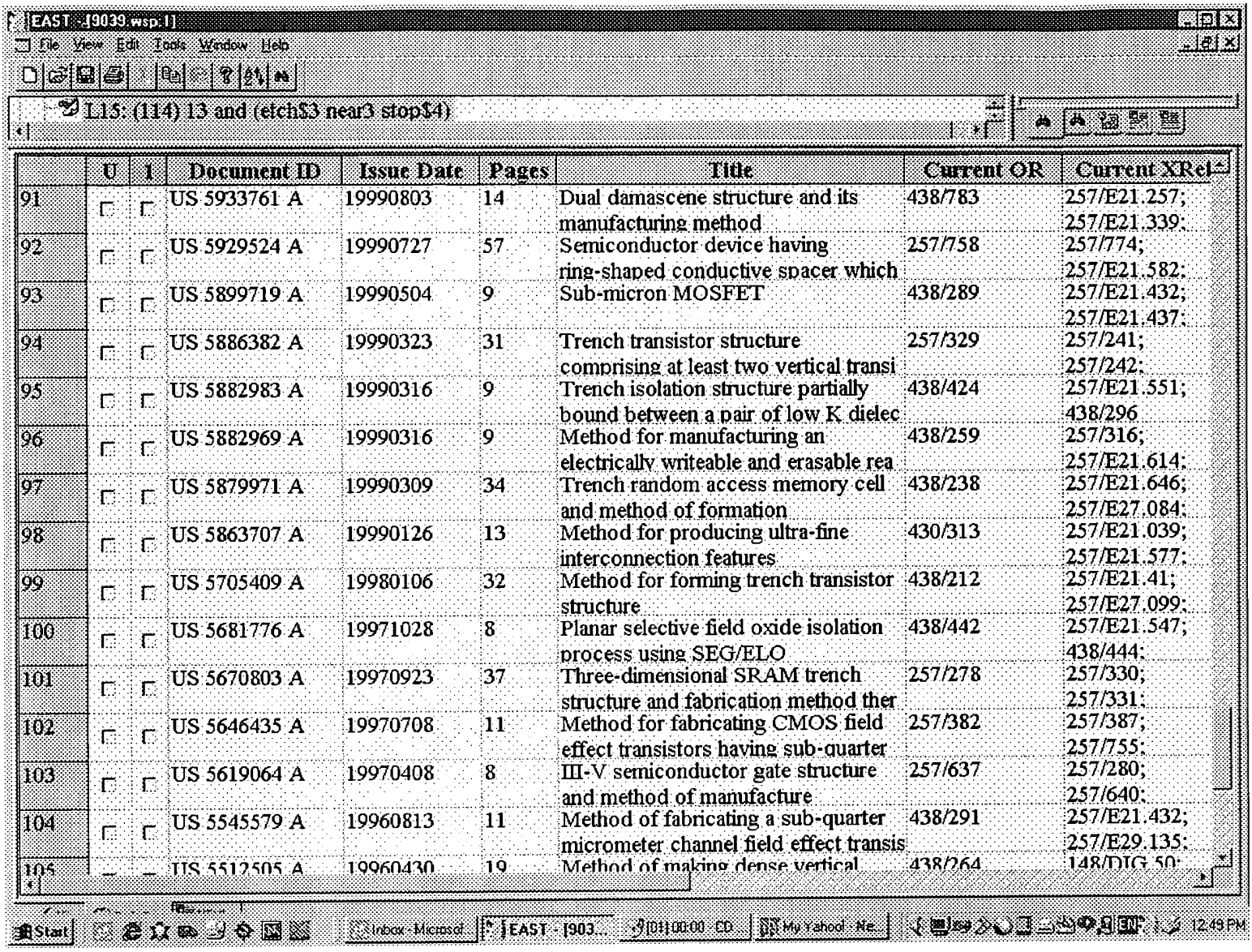
76	☐	☐	US 6174763 B1	20010116	36	Three-dimensional SRAM trench structure and fabrication method ther	438/238	257/E21.661; 257/E21.703;
77	☐	☐	US 6153905 A	20001128	22	Semiconductor component including MOSFET with asymmetric gate electr	257/320	257/316; 257/317;
78	☐	☐	US 6097076 A	20000801	19	Self-aligned isolation trench	257/513	257/510; 257/524;
79	☐	☐	US 6096594 A	20000801	11	Fabricating method of a dynamic random access memory	438/238	257/E21.648; 438/252;
80	☐	☐	US 6091129 A	20000718	44	Self-aligned trench isolated structure	257/510	257/622; 257/E21.206;
81	☐	☐	US 6087705 A	20000711	9	Trench isolation structure partially bound between a pair of low K dielec	257/510	257/501; 257/644;
82	☐	☐	US 6074955 A	20000613	9	Method of fabricating a node contact window of DRAM	438/710	257/E21.507; 257/E21.577;
83	☐	☐	US 6066555 A	20000523	17	Method for eliminating lateral spacer erosion on enclosed contact topogra	438/634	257/E21.582; 438/637;
84	☐	☐	US 6051456 A	20000418	24	Semiconductor component and method of manufacture	438/202	257/E21.696; 257/E27.015;
85	☐	☐	US 6043131 A	20000328	7	Method for making a flower shaped DRAM capacitor	438/396	257/E21.012; 257/E21.016;
86	☐	☐	US 6037202 A	20000314	33	Method for growing an epitaxial layer of material using a high temperature in	438/212	257/E21.41; 257/E27.099;
87	☐	☐	US 6037194 A	20000314	27	Method for making a DRAM cell with grooved transfer device	438/147	257/E21.655; 438/175
88	☐	☐	US 5963279 A	19991005	32	Liquid crystal display device containing openings in a protective la	349/54	257/E21.703; 257/E27.111;
89	☐	☐	US 5945707 A	19990831	25	DRAM cell with grooved transfer device	257/330	257/331; 257/E21.655
90	☐	☐	US 5942803 A	19990824	7	Methods for forming openings with	257/774	257/E21.579;



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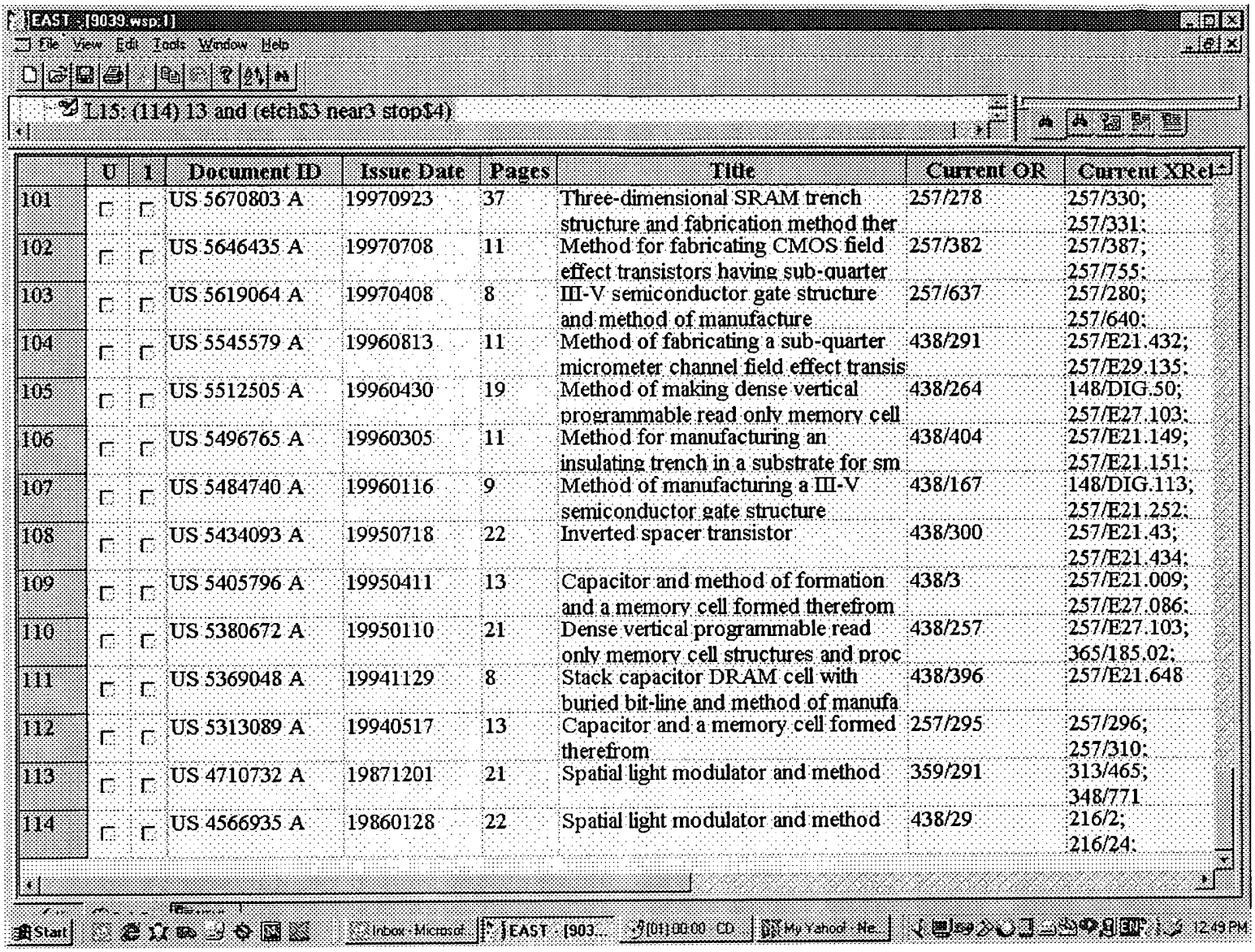
91	☐	☐	US 5933761 A	19990803	14	Dual damascene structure and its manufacturing method	438/783	257/E21.257; 257/E21.339;
92	☐	☐	US 5929524 A	19990727	57	Semiconductor device having ring-shaped conductive spacer which	257/758	257/774; 257/E21.582;
93	☐	☐	US 5899719 A	19990504	9	Sub-micron MOSFET	438/289	257/E21.432; 257/E21.437;
94	☐	☐	US 5886382 A	19990323	31	Trench transistor structure comprising at least two vertical transi	257/329	257/241; 257/242;
95	☐	☐	US 5882983 A	19990316	9	Trench isolation structure partially bound between a pair of low K dielec	438/424	257/E21.551; 438/296
96	☐	☐	US 5882969 A	19990316	9	Method for manufacturing an electrically writeable and erasable rea	438/259	257/316; 257/E21.614;
97	☐	☐	US 5879971 A	19990309	34	Trench random access memory cell and method of formation	438/238	257/E21.646; 257/E27.084;
98	☐	☐	US 5863707 A	19990126	13	Method for producing ultra-fine interconnection features	430/313	257/E21.039; 257/E21.577;
99	☐	☐	US 5705409 A	19980106	32	Method for forming trench transistor structure	438/212	257/E21.41; 257/E27.099;
100	☐	☐	US 5681776 A	19971028	8	Planar selective field oxide isolation process using SEG/ELO	438/442	257/E21.547; 438/444;
101	☐	☐	US 5670803 A	19970923	37	Three-dimensional SRAM trench structure and fabrication method ther	257/278	257/330; 257/331;
102	☐	☐	US 5646435 A	19970708	11	Method for fabricating CMOS field effect transistors having sub-quarter	257/382	257/387; 257/755;
103	☐	☐	US 5619064 A	19970408	8	III-V semiconductor gate structure and method of manufacture	257/637	257/280; 257/640;
104	☐	☐	US 5545579 A	19960813	11	Method of fabricating a sub-quarter micrometer channel field effect transis	438/291	257/E21.432; 257/E29.135;
105	☐	☐	US 5512505 A	19960430	19	Method of making dense vertical	438/264	148/DIG.50;



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101	☐	☐	US 5670803 A	19970923	37	Three-dimensional SRAM trench structure and fabrication method ther	257/278	257/330; 257/331;
102	☐	☐	US 5646435 A	19970708	11	Method for fabricating CMOS field effect transistors having sub-quarter	257/382	257/387; 257/755;
103	☐	☐	US 5619064 A	19970408	8	III-V semiconductor gate structure and method of manufacture	257/637	257/280; 257/640;
104	☐	☐	US 5545579 A	19960813	11	Method of fabricating a sub-quarter micrometer channel field effect transis	438/291	257/E21.432; 257/E29.135;
105	☐	☐	US 5512505 A	19960430	19	Method of making dense vertical programmable read only memory cell	438/264	148/DIG.50; 257/E27.103;
106	☐	☐	US 5496765 A	19960305	11	Method for manufacturing an insulating trench in a substrate for sm	438/404	257/E21.149; 257/E21.151;
107	☐	☐	US 5484740 A	19960116	9	Method of manufacturing a III-V semiconductor gate structure	438/167	148/DIG.113; 257/E21.252;
108	☐	☐	US 5434093 A	19950718	22	Inverted spacer transistor	438/300	257/E21.43; 257/E21.434;
109	☐	☐	US 5405796 A	19950411	13	Capacitor and method of formation and a memory cell formed therefrom	438/3	257/E21.009; 257/E27.086;
110	☐	☐	US 5380672 A	19950110	21	Dense vertical programmable read only memory cell structures and proc	438/257	257/E27.103; 365/185.02;
111	☐	☐	US 5369048 A	19941129	8	Stack capacitor DRAM cell with buried bit-line and method of manufa	438/396	257/E21.648
112	☐	☐	US 5313089 A	19940517	13	Capacitor and a memory cell formed therefrom	257/295	257/296; 257/310;
113	☐	☐	US 4710732 A	19871201	21	Spatial light modulator and method	359/291	313/465; 348/771
114	☐	☐	US 4566935 A	19860128	22	Spatial light modulator and method	438/29	216/2; 216/24;